Abstract

A processor includes controller circuitry operative to control the performance of a continuity check for each of a plurality of flows of protocol data units (PDUs) received by the processor. The controller circuitry is further operative to control access to a set of continuity check counters comprising a counter for each of the plurality of flows. The processor stores an identifier for each of a subset of the plurality of flows in a continuity check cache, and determines if a given flow for which a PDU is received in the processor has a corresponding entry in the continuity check cache. If the given flow has such an entry, the processor prevents a corresponding one of the continuity check counters from being updated, and if the given flow does not have such an entry, the processor clears the corresponding one of the continuity check counters and stores a flow identifier for the given flow in the continuity check cache.